61 THE CHIPS TO SYSTEMS CONFERENCE

SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
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Generative-AI Technology for block and SoC IR closure:

Root-Cause and Repair strategies

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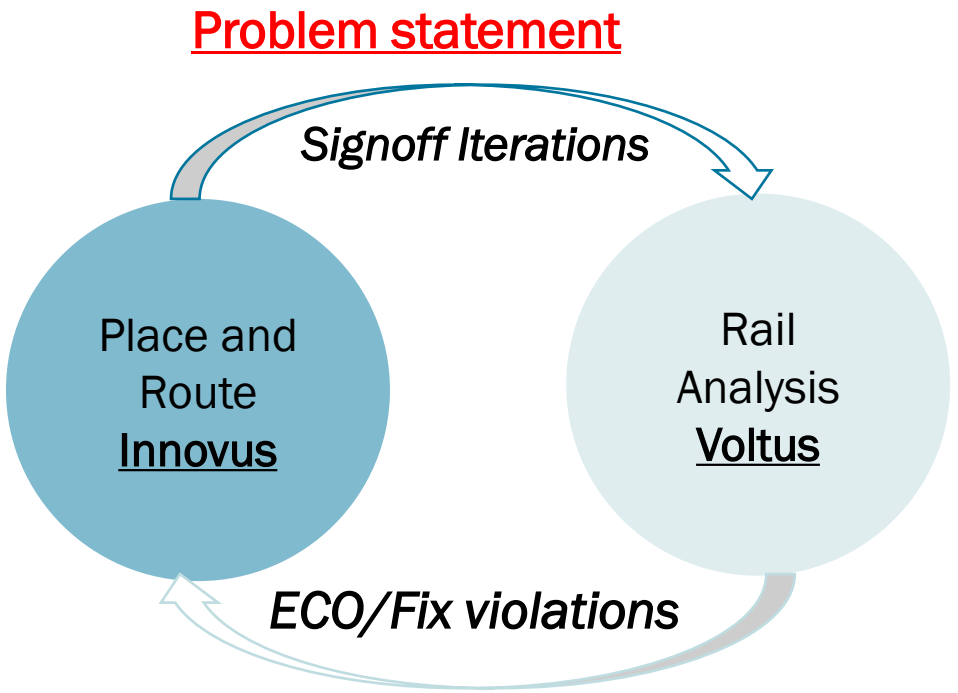
Agenda

- Problem Statement
- Intelligence – Brief overview
- IR fixing techniques
- Implementation flow
- Considerations and Results
- Conclusion

Goal: Today's methodology of IR-fixing which is mostly a manual process takes multiple weeks per block, with the discussed methodology IR fixing can be brought down to less than a day with high (>90%) fix-rate



Intelligence Process

LEARN

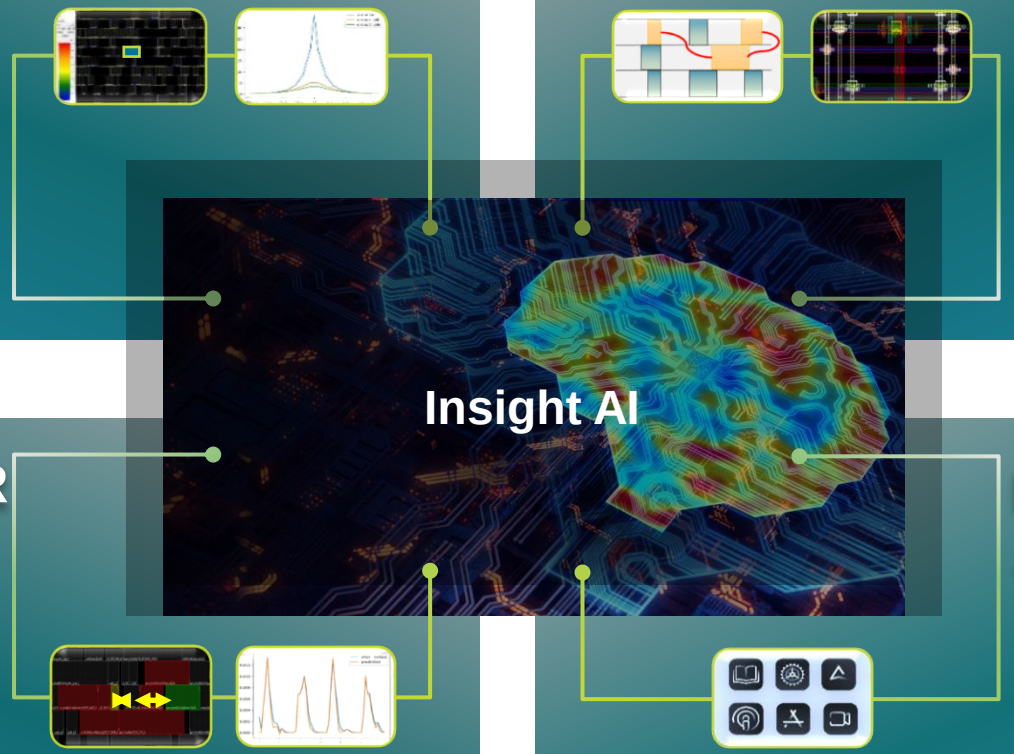
1

- **AI modeling** of the power grid right at the onset of design
- AI-based IR fixing engine learned from various fixing methods/strategies

IMPROVE

3

- **DRC and timing aware automated** fixing built-in during the design process
- AI guided multi-method fixing enabled by placement, routing, ECO, etc.



DISCOVER

- Industry's **first AI-based fast IR** inference capability for hotspot detection
- Fast root cause discovery of aggressors, victims and grid-based feedback

2

EMPOWER

- **Build custom applications** to help mitigate IR problems across the design flow
- Enable customers to improve PPA through better PG design

4

1 : Learn (Fast Analysis)

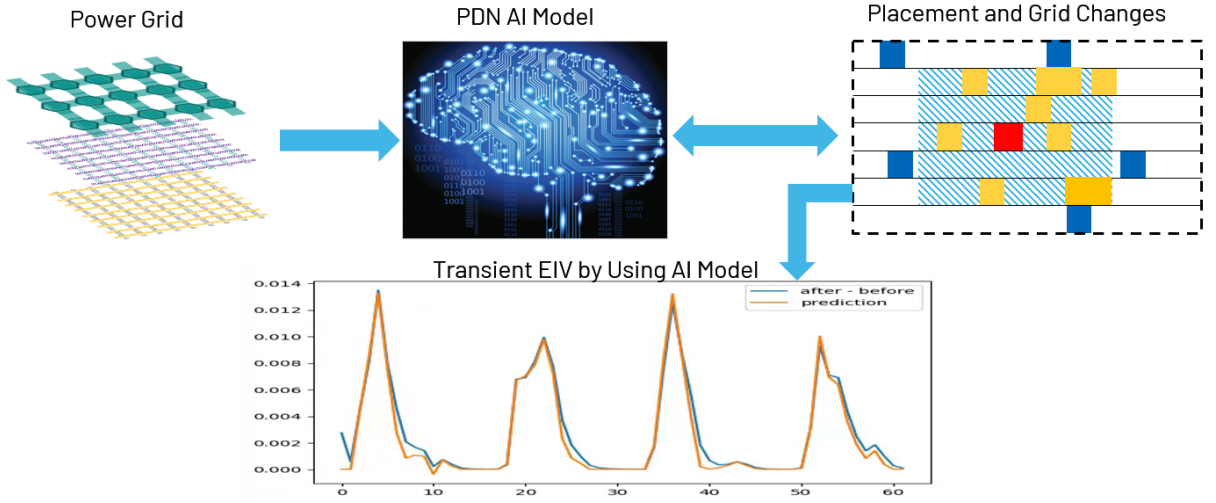
- Leverages proprietary neural networks to build models of the power grid
- Performs extremely fast incremental IR analysis
- Summarize feedback on the impact of design changes

2 : Discover (Diagnostics)

- Analyses Input from IRA (Electrical, Spatial and Timing factors for predicting IR drop issues)
- Uses Deep learning to discover the root cause of IR Drop problems
- Identify Aggressors, Victims and Resistance bottlenecks

3/4 : Improve (Multi-Method)/ Empower

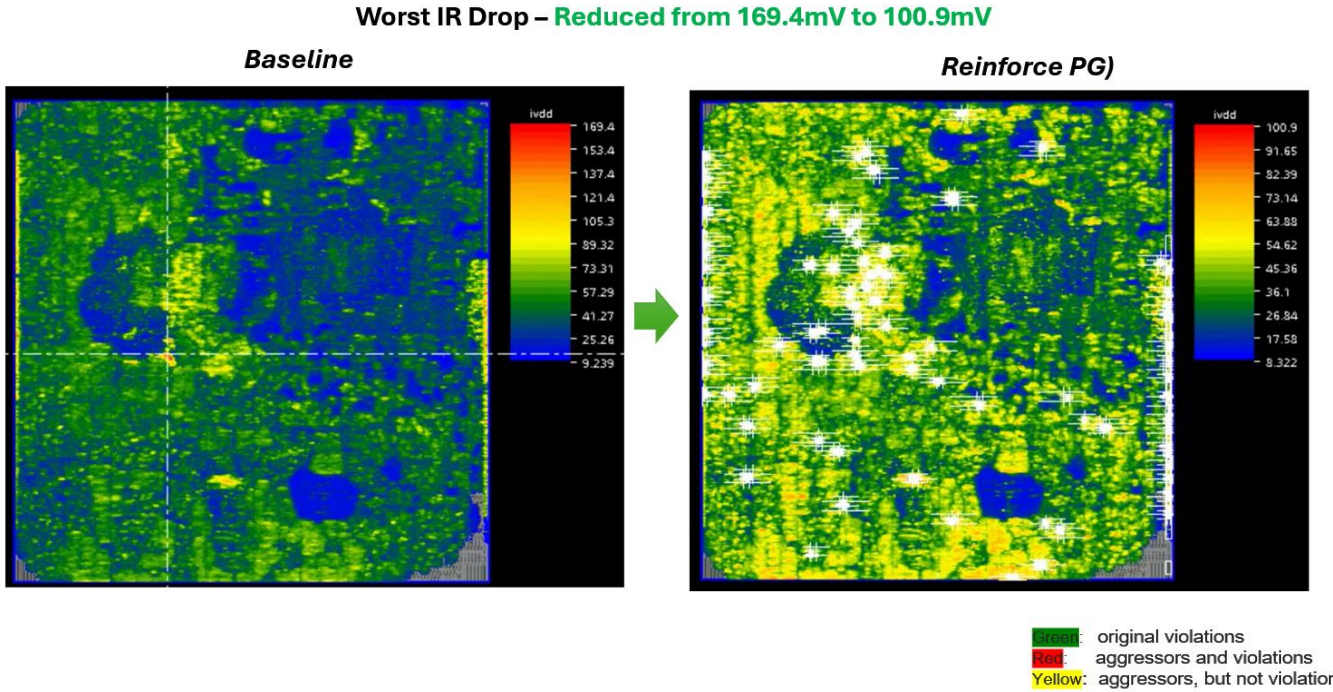
- Precise fixing methods: Better utilization & improved PPA
- Utilizes decision-tree methods (Timing and DRC aware): placement, grid reinforcement, routing, and ECOs



IR Fix Techniques

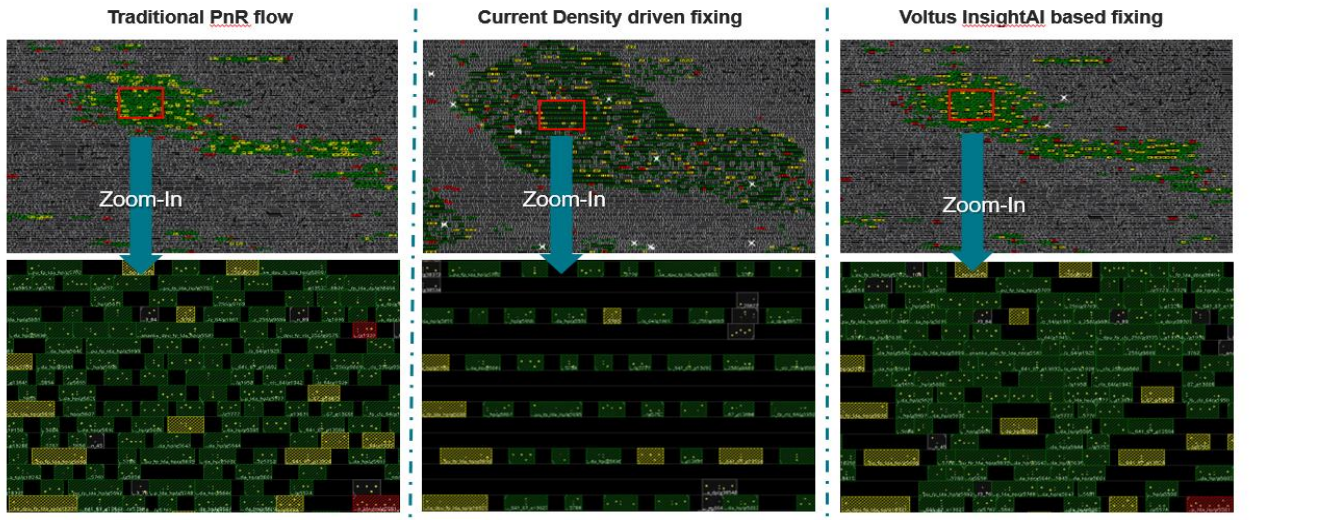
Reinforce PG (RPG)

- IR drop hot spot spans several rows and columns of PG sets dominated by registers / Clock cells (Cannot move much)
- Placement spreading alone cannot solve this hot spot
- Improve the power delivery on existing Power Grid - **Need local PG Addition**

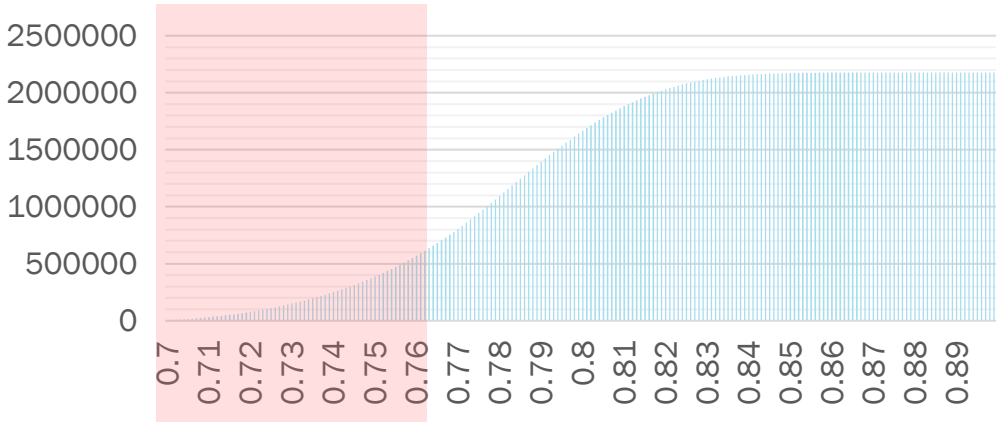


IR Aware placement

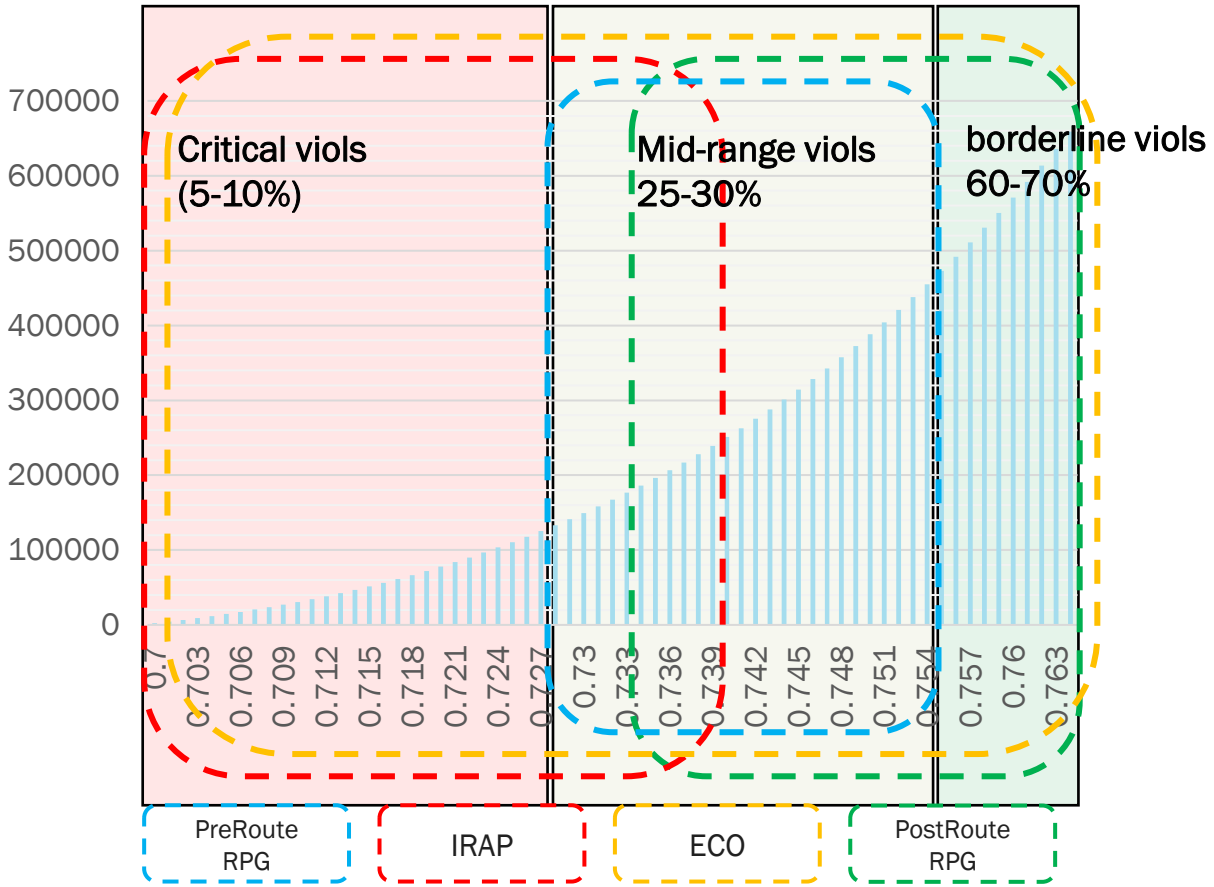
- Spreads “hot spots” to reduce IR drop – Effective for prevention of hot spots (especially due to Register / ICG clustering)
- Spread hotspots + Apply padding to high current density instances for better IR prevention + fixing



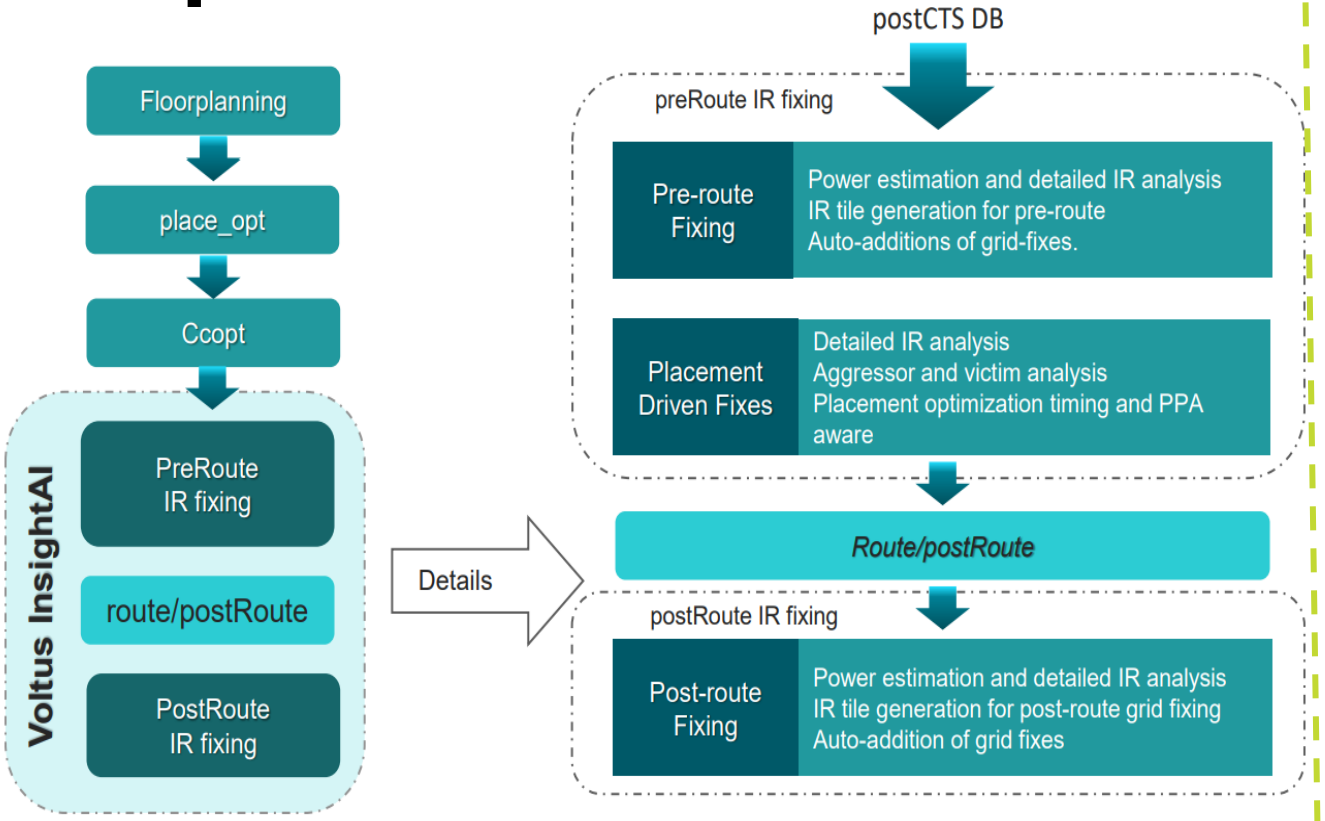
Cost functions for violation binning



- Repair range
  - PreRoute RPG : low and mid range (blue)
  - IRAP : high and mid range (red)
  - PostRoute RPG: low and mid range (green)
  - ECO : entire range (yellow)
- Predictability in terms of IR-fixing
  - PreRoute RPG > PostRoute RPG > IRAP ~ ECO
- PPA cost
  - IRAP > PreRoute RPG > PostRoute RPG > ECO



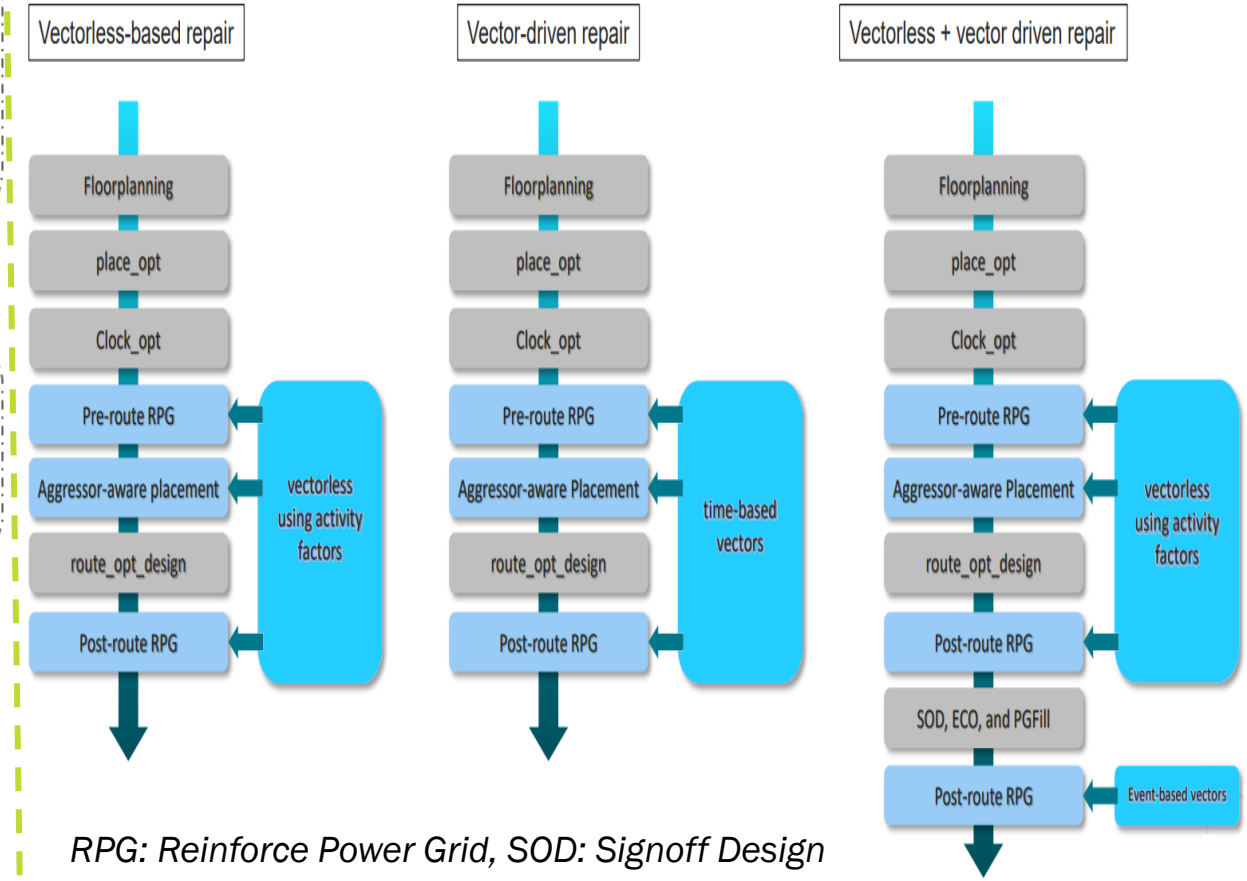
Implementation flow



Types of analysis/repair flow:

- Vectorless analysis and IR fix
- Vector based/driven IR fix
- Both Vectorless+Vector based flow

- IR Threshold Limit (%)
- In IR fix stage such as
  - PreRoute
  - PostRoute
  - ECO



RPG: Reinforce Power Grid, SOD: Signoff Design
ECO: Engineering Change order

IR Setup variation:

In effort levels for IR fixing

- Reinforce PG
- IR aware placement
- Auto IR fix
- Timing aware

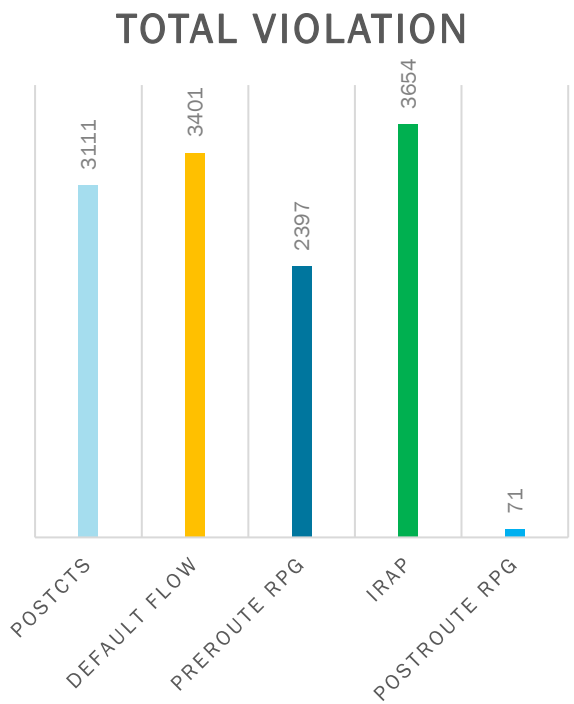
Design Types:

1. Analog on Top (AoT)
2. Digital on Top (DoT)
3. Hierarchical Design
4. Low Power design

Results – Test case 1

Design Information:

- Technology: 5nm
- Design Size: 1.14Million
- Analysis type: Vectorbased
- Domain threshold: 0.825V



		postCts	Traditional (no IR fix) Flow	Insight AI Summary			
				PreRoute RPG	IRAP	routeOpt	postRoute RPG
Utilization [%]			57.785	57.590	57.590	57.746	57.746
Runtime (HH:MM)			18:30	1:12	0:55	8:40	4:05
Timing	WNS [ns]		-0.493				-0.416
	TNS [ns]		-1004.1				-1104.0
	NVP		15096				16440
IR	WIV [mV]	93.21	86.91	88.18	86.87		18.413
	TIV [mV]	30702	32087	22205	22122		403.2
	NVIV	3111	3401	2397	2654		71
Power [mV]	Total	666.27	680.55	666.27	677.43		677.48
	Internal	254.82	257.11	254.82	256.26		256.27
	Switching	382.51	394.21	382.51	392.12		392.17
	Leakage	16.68	16.22	16.68	16.16		16.16

78.8%

98.7%

97.9%

Observations:

- ✓ No difference in design utilization
- ✓ 97.9% IR fix rate in single iteration
- ✓ No timing impact
- ✓ No significant difference in DRC summary
- ✓ Negligible total power increase

RPG – Reinforce Power Grid, IRAP – IR aware placement,
WNS – Worst Negative Slack, TNS – Total Negative Slack, NVP – Number of Violation paths
WIV – Worst Instance Voltage drop, TIV – Total Instance Voltage drop, NVIV – Number of Violation Instance Voltage drop

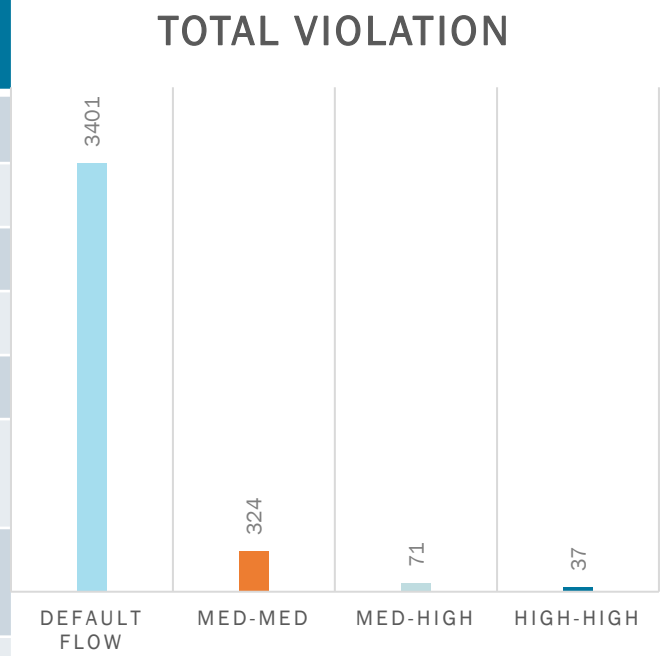
Results – Test case 2

Design Information:

- Technology: 5nm
- Design Size: 1.99M
- Analysis type:

  Vectorbased & dynamic
- Supply voltage: 0.825V
- Domain threshold: 10%

		Traditional (no IR fix) Flow	Insight AI Summary (effort: preroute_rpg_effort : irap_effort : pro_auto_ir_fix_effort : pro_timing_aware_effort)		
			L:M:M:L	L:M:H:L	L:H:H:L
Utilization [%]		58.203	57.745	57.745	57.746
DRCs		257	228	236	300
Runtime (HH:MM)		18:30	15:12	14:52	19:54
Timing	WNS [ns]	-1.225	-1.199	-1.199	-1.189
IR	WIV [mV]	86.91	25.24 (70.9%)	18.413 (78.8%)	13.10 (84.9%)
	TIV [mV]	32087	1883 (94.1%)	403.2 (98.7%)	122.39 (99.6%)
	NVIV	3401	324 (90.4%)	71 (98.7%)	37 (98.9%)
Power	Total [mV]	680.55	677.39	677.39	677.37



Observations:

- ✓ >90% IR fix rate based different strategies
- ✓ IR fix effort increase
  - IR fix rate increase
  - moderate DRC increase and easy to fix
  - moderate runtime difference
- ✓ No significant difference of power and timing based different strategies

preroute_rpg_effort: IR fix effort of reinforce-pg during preroute stage
irap_effort: IR fix effort of ir aware placement during preroute stage
pro_auto_ir_fix_effort: IR fix effort of reinforce-pg during postroute stage
pro_timing_aware_effort: Timing aware effort during postroute reinforce-pg

Results – Test case 3

Design Information:

Technology: 5nm

Design Size: Block (100K)

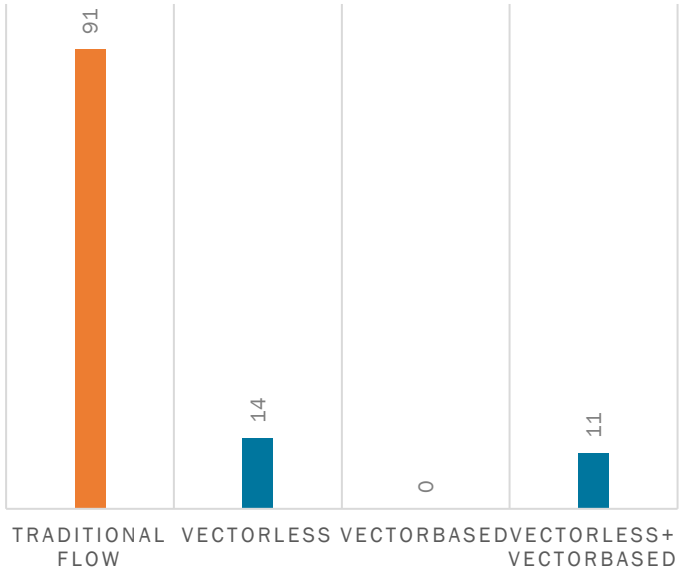
Analysis type:

Vectorless/Vectorbased & Dynamic

Supply voltage: 0.935V

Effort: H:H:H:L

Domain threshold: 10%



		Vectorless-dynamic		Vectorbased-dynamic		Vectorless+ Vectorbased
		Traditional (no IR fix) Flow	Insight AI Summary	Traditional (no IR fix) Flow	Insight AI Summary	Insight AI Summary
Utilization [%]		88.087	87.587	88.087	87.748	87.79
DRCs		13	24	13	15	17
Runtime (HH:MM)		0:57	1:16	0:57	1:23	1:30
Timing	WNS [ns]	-0.011	-0.008	-0.011	-0.010	-0.010
IR	WIV [mV]	76.454	14.953 (80%)	79.049	0	17.159
	TIV [mV]	2426.02	131.324 (95%)	1627.09	0	112.64
	NVIV	91	14 (82%)	33	0 (100%)	11
Power	Total [mV]	7.72	7.67	5.82	5.82	

Observations:

- ✓ IR fix rate difference based different analysis type
  IR violation type, IR violation numbers, IR violation location
- ✓ Moderate run time difference
- ✓ Moderate difference in DRC summary
- ✓ No significant difference in total power and timing increase

RPG – Reinforce Power Grid, IRAP – IR aware placement,
WNS – Worst Negative Slack, TNS – Total Negative Slack, NVP – Number of Violation paths
WIV – Worst Instance Voltage drop, TIV – Total Instance Voltage drop, NVIV – Number of Violation Instance Voltage drop

Results – Test case 4

Design Information:

Technology: 5nm

Design Size: 500K

Analysis type:

Vectorless & Dynamic

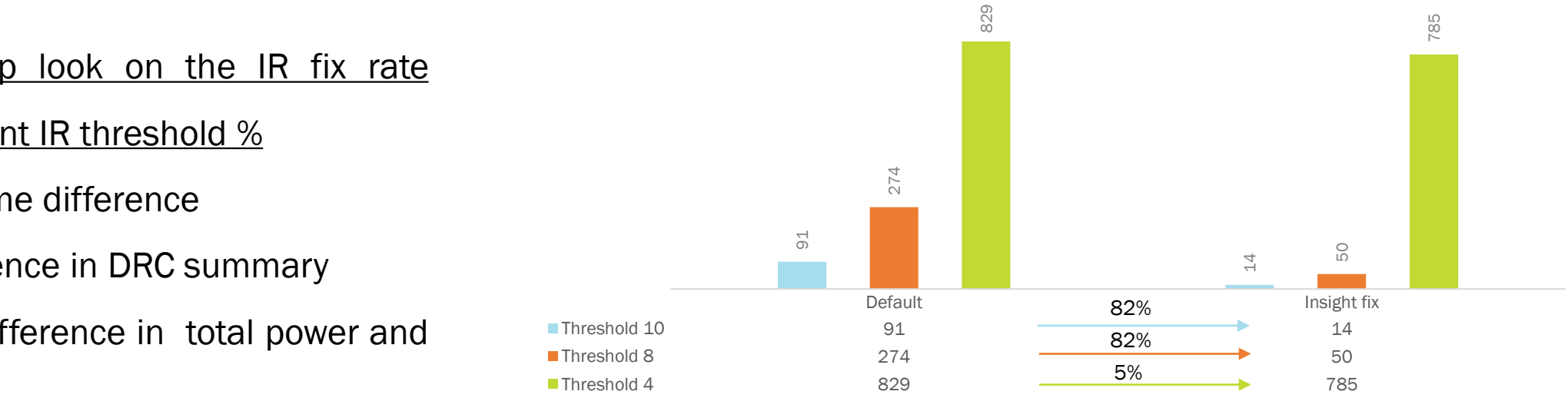
Supply voltage: 0.935V

Effort: H:H:H:L

		Pre IR fix	Insight Summary	Pre IR fix	Insight Summary	Pre IR fix	Insight Summary
IR threshold [%]		10	10	8	8	4	4
IR Postroute_rpg	WIV [mV]	76.454	14.953 (80%)	129.317	34.7	166.717	59.6352
	TIV [mV]	2426.02	131.324 (95%)	6160.09	558.548	31193.8	10095.6
	NVIV	91	14 (82%)	274	50 (82%)	829	785 (5%)

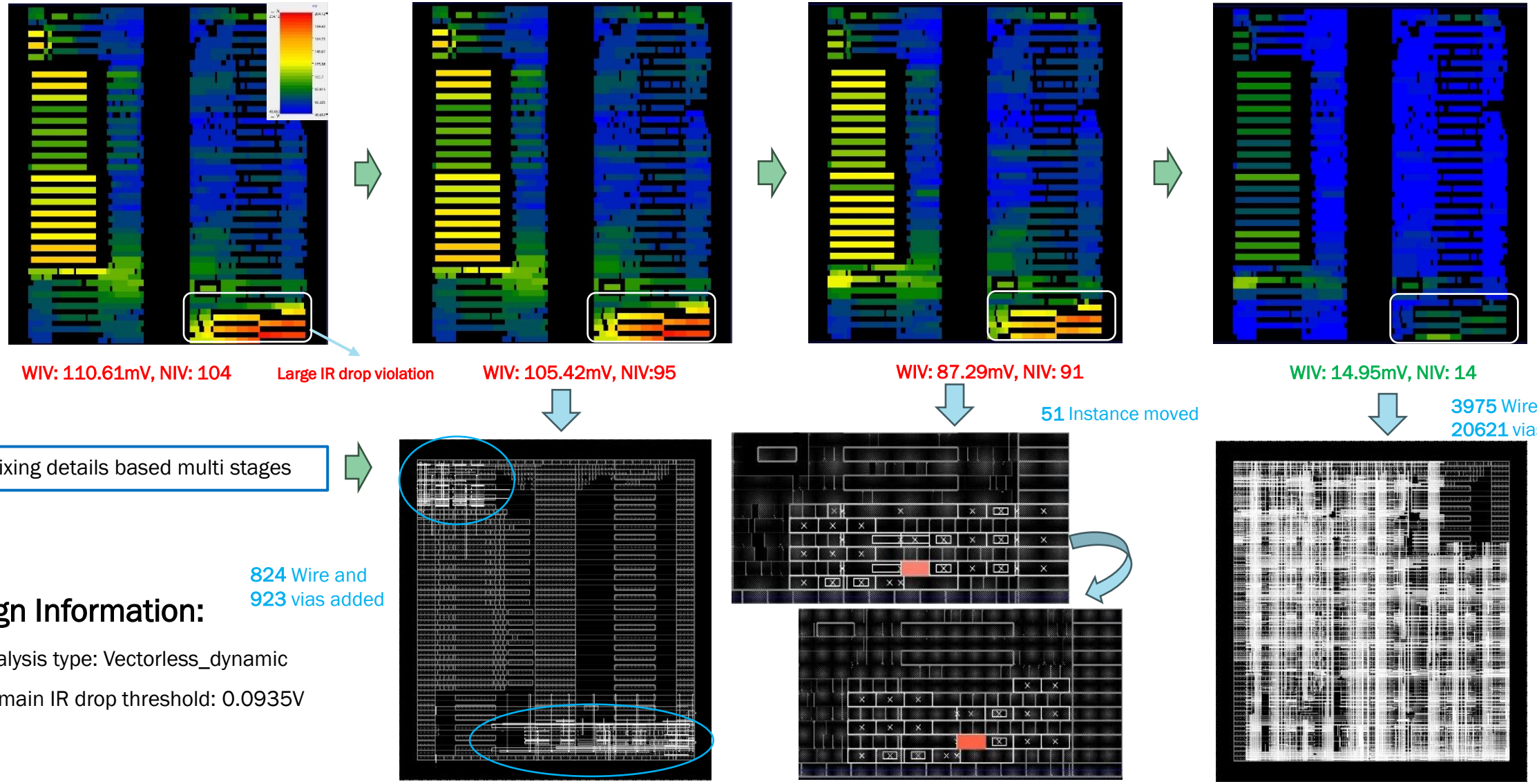
Observations:

- ✓ Provides a deep look on the IR fix rate based on different IR threshold %
- ✓ Moderate run time difference
- ✓ Moderate difference in DRC summary
- ✓ No significant difference in total power and timing increase



Fix techniques – Stage (Pre/Post Route)

Instance voltage drop



Design Information:

- Analysis type: Vectorless_dynamic
- Domain IR drop threshold: 0.0935V

Summary

- From the results, the technology has proven the capability to predict early-stage IR drop issues with improved PPA consistently
- The proposed flow helps improve time to market (TTM) by enabling fast and automated IR drop closure, improved productivity, and better PPA (>97% fix rate in multiple advance technology designs)
- It seamlessly integrates/adapts with implementation and signoff flow to enable timing and DRC aware fixes to the design
- With the breakthrough capabilities of Insight AI, designers can overcome the immense challenge of designing robust PDN and unlock the full potential of advanced node technologies